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CS 5780

Lab2 – Post Lab

1. Why can't both pins PA0 and PC0 be used for external interrupts at the same time?

It is because they are grouped on a single multiplexer with the output routed to the EXTI0 input. Because only a single pin from a group can be used, the chosen pins are such that they conﬂict with each other when using multiple external interrupts.

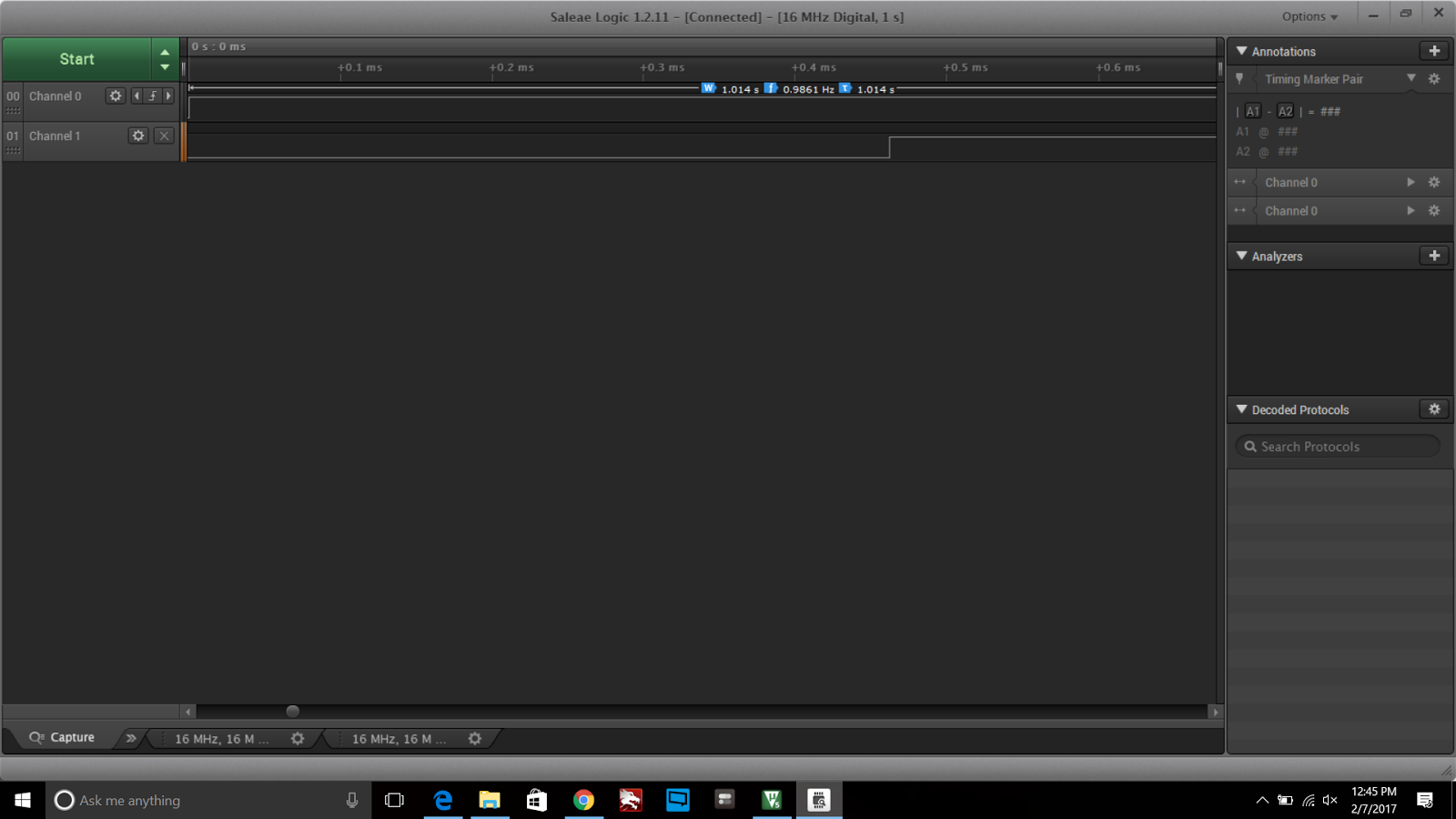
1. What software priority level gives the highest priority, what level gives the lowest?

0 gives the highest priority and 4 gives the lowest priority.

1. How many bits does the NVIC have reserved in its priority (IPR) registers for each interrupt? (including non-implemented bits)
   * Which bits in the group are implemented?

It only has 1 bit reserved for each interrupt. The MR0 bit was used in this lab for the push down button.

1. What was the latency between pushing the Discovery board button and the LED change (interrupt handler start) that you measured with the logic analyzer?
   * Make sure to include a screenshot in the post-lab submission.



The latency is about 0.4631 ms from rising edge to rising edge.

1. Why do you need to clear status flag bits in peripherals when servicing their interrupts?

Unless the corresponding pending flags are cleared the corresponding interrupt is enabled, so the EXTI interrupt handler will be repeatedly called.